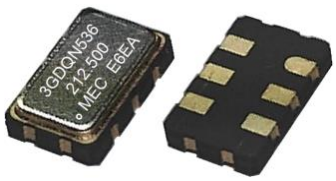
Low Jitter Differential VCXOs — LVDS Differential

GDQN _ _	LVDS Differential	0.6 ps RMS Jitter	SMD	2.5 V	3.3 V	Min. 10 MHz	Max. 1,500 MHz

Features

Mercury's Low Jitter Differential VCXO, with low current consumption (22 mA for LVDS 622.080 MHz at 3.3V) & an integrated phase jitter performance of 0.6pS RMS. Gaining its precision frequency control market position by providing engineers with *few days* samples for prototypes and low cost, fast delivery for volume production. The perfect solution to replace traditional XO's & VCXO's that use a more expensive highfrequency, fundamental crystal and a noisy PLL multiplier circuit.



General specifications , at Ta=+25°C , CL=15pF

Model	GDQN								
Available Frequency Range	10 ~ 1,500 MHz								
Supply Voltage V_{DD} (code)	+ 2.5 V_{DD} ± 5 % (voltage code ' 25 ')			+ 3.3 V_{DD} ± 5 % (voltage code ' 33 ')					
Current with Output Disable	16 mA typical								
Current Consumption (V_{DD} = + 2.5 V)	100 MHz : 16 mA	250 MHz : 18 mA	500 MHz : 21 mA	750 MHz : 22 mA	1,000 MHz : 24 mA	1,350 MHz : 26 mA			
Current Consumption (V_{DD} = + 3.3 V)	100 MHz : 25 mA	250 MHz : 30 mA	500 MHz : 35 mA	750 MHz : 39 mA	1,000 MHz : 43 mA	1,350 MHz : 47 mA			

Frequency Stability Codes	Frequency Stability over Operating Temperature Range	± 25 ppm	± 50 ppm	± 100 ppm	If non-standard , please enter the desired stability after the " C " or " I " represents . For example : " C20 " ± 20 ppm over -10°C to +70°C ; " I20 " ± 20 ppm over -40°C to +85°C
	Commercial (-10°C to +70°C)	A	B	C	
	Industrial (-40°C to +85°C)	D	E	F	

Output Logic " High " , " 1 "	1.4 V typical ; 1.6 V max.	Output Logic " Low " , " 0 "	0.9 V min. ; 1.1 V typical.
Load	100 Ω between output and complimentary output	Rise Time / Fall Time	0.4 ns. (max.) [20% ↔ 80% waveform]
Duty Cycle	50 % ± 5%	Aging at Ta = +25°C	± 5 ppm max. for first year at 25°C
Start-up Time	10 m sec. (max.)	Storage Temperature	-55°C to + 150°C

SSB Phase Noise [dBc / Hz (typical)]	Offset	77.76	122.88	125	156.25	212.5	491.52	622.08	1000	1250
	10 Hz	-74	-68	-69	-67	-53	-56	-51	-46	-32
	100 Hz	-104	-98	-97	-92	-86	-87	-77	-80	-68
	1 KHz	-121	-114	-114	-112	-109	-101	-99	-96	-94
	10 KHz	-130	-123	-124	-121	-118	-110	-109	-105	-103
	100 KHz	-134	-127	-129	-124	-121	-113	-114	-108	-105
	1 MHz	-140	-138	-136	-136	-133	-125	-121	-116	-117
	10 MHz	-157	-155	-154	-153	-151	-143	-141	-135	-136
Phase Jitter (12KHz ~ 20 MHz, RMS) unit : ps.		0.5	0.6	0.5	0.6	0.6	0.6	0.5	0.7	0.6

Control Voltage Function on Pad 1

Supply Voltage (V_{DD})	V_{DD} = +2.5 V ; Vcon Center = +1.25V	V_{DD} = +3.3 V ; Vcon Center = +1.65V
Vcontrol Range	+ 0.2V ~ +2.3V	+ 0.3V ~ +3.0V
Frequency Pulling Range	± 80 ppm (min.)	± 80 ppm (min.)
	Up to ± 200 ppm (min.) is also available. Please contact Mercury.	
Absolute Voltage	2.8 V max. for 2.5V V_{DD}; 4.0 V max. for 3.3V V_{DD}	

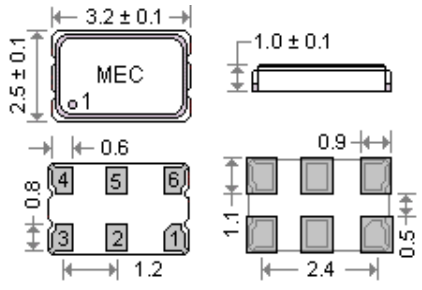
Linearity	± 5% typical. ±10% (max.)	Input Impedance	1 MΩ typical
Transfer Function	Positive Transfer	Bandwidth	10 KHz min. Measured at -3 dB

Output Enable Function

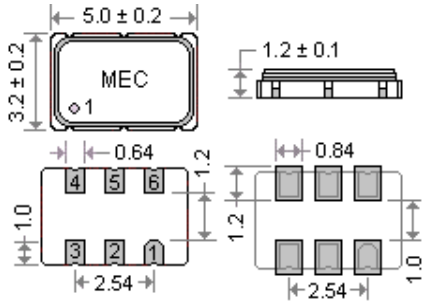
OE Control on Pad 2	70% of V_{DD} (min.) to enable output. (Open connection prohibit)
	30% of V_{DD} (max.) to disable output.
Output Enable Time / Disable Time	200 ns. Max. / 50 ns. Max.

Outline Dimensions (Unit : mm) , Suggested pad Layout for SMDs

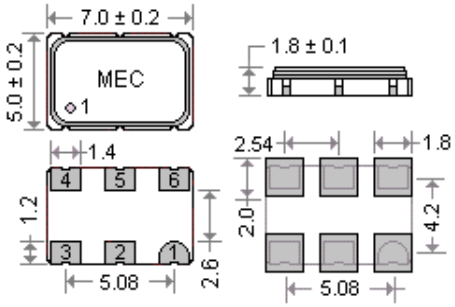
GDQN326



GDQN536



GDQN576



Pad Connections

Pad 1 : VCXO ; **Pad 2 :** OE: High Enable ; **Pad 3 :** Ground
Pad 4 : Differential ; **Pad 5** : Complementary ; **Pad 6** : Supply Voltage

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Voltage Controlled Crystal Oscillators [VCXO]

GTQN	GPQN	GDQN	Q family / N series	SMD	2.5 V	3.3 V
CMOS waveform	**PECL** Differential	**LVDS** Differential				

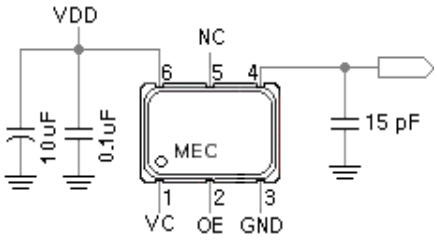
Part Number Format and Example

Example : 3GPQN576 - E - 100N - 622.080

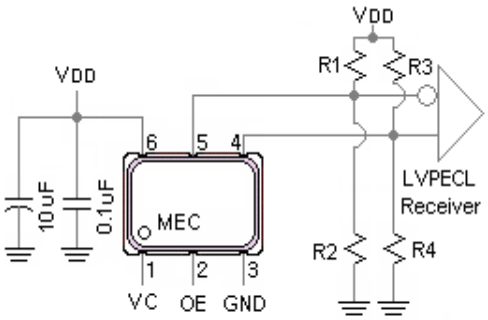
3	GPQN	576	-	E	-	100N	-	622.08
Supply Voltage " **3** " for 3.3V " **25** " for 2.5V	GTQN : CMOS GPQN : PECL GDQN : LVDS	Package Size " **576** " : 7x5 mm " **536** " : 5x3.2 mm		Frequency Stability Code " **E** " : ± 50 ppm over -40 to +85°C Other frequency stabilities are available.		±100 ppm (min.) frequency pulling range		Frequency (MHz)

Test Circuits and Output Waveforms

CMOS Test Circuit

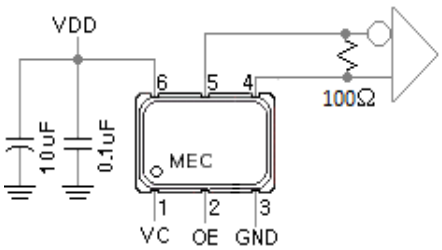


PECL Test Circuit

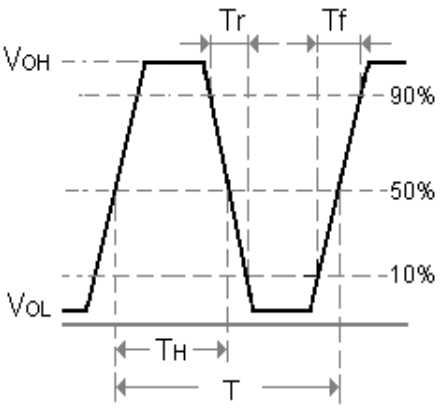


V_{DD} = 3.3V ; R1 = R3 = 127 Ω ; R2 = R4 = 82.5 Ω
V_{DD} = 2.5V ; R1 = R3 = 250 Ω ; R2 = R4 = 62.5 Ω

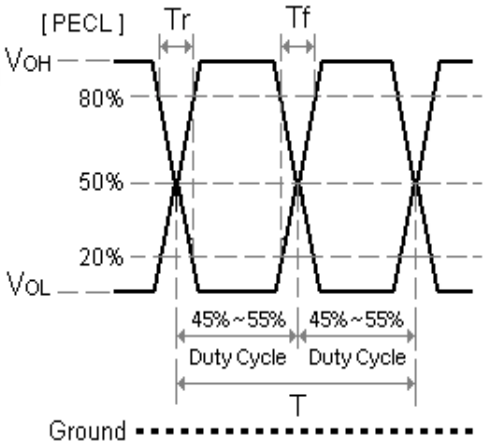
LVDS Test Circuit



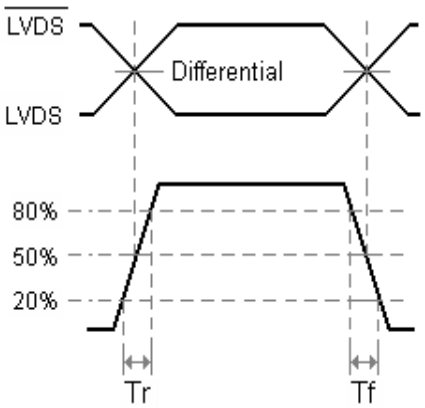
CMOS Output Wave Form



PECL Output Wave Form



LVDS Output Wave Form



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